AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION

Please replace the title with the following rewritten title.

-- DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM --

Please replace the paragraph beginning at page 2, line 1, with the following rewritten paragraph.

-- Programs, however, are produced at the same time as the devices they are applied to are developed. Many programs are produced while the devices are still unfinished. Further, after the devices are produced, modifications in their specifications sometimes ~~causes~~ cause part of the control programs produced up to then and stored in the microcomputers to no longer match with the devices. Further, in a large-scale system, the programs are also large in size, so it is difficult to find all the defects in the programs only by tests before production. In many cases, the bugs in the programs are found after production. --

Please replace the paragraph beginning at page 2, line 13, with the following rewritten paragraph.

-- When bugs are found after the production of a microcomputer, since the programs cannot be modified, the manufactured microcomputers cannot be used and become wasted and a

~~cause~~ loss. Further, even if producing debugged programs and newly ordering and producing the microcomputers, there are drawbacks in cost and time. --

Please replace the paragraph beginning at page 15, line 18, with the following rewritten paragraph.

-- The CPU 10 reads instruction codes from the ROM 30 according to a not illustrated program counter and performs operations and other processing accordingly. Further, the CPU 10 is provided with an interrupt processing function performing a predetermined interrupt processing in response to an interrupt request signal ~~SA~~ S_A from the outside. --

Please replace the paragraph beginning at page 15, line 25, with the following rewritten paragraph.

-- In the present invention, the buggy program is processed utilizing the interrupt processing function of the CPU 10. Note that~~,~~ the interrupt processing function is utilized for immediately processing in response to a request signal input from the outside during the execution of a normal program. Generally, plural interruptions that can be processed ~~processable~~ by the CPU 10 are assigned to each external interrupt request. For this reason, by utilizing an interrupt processing not utilized in the normal processing, for example, the abort interruption provided for testing the microcomputer, the debugged program is able to be executed without affecting the normal interrupt processing. --

Please replace the paragraph beginning at page 17, line 20, with the following rewritten paragraph.

-- When the CPU 10 is executing the program, the count of the program counter is output to the address bus ADRBUS as the program address. The coincidence detecting circuit 120 compares the program address input from the address bus with the bug address set in the bug address setting register 110 and generates the interrupt request signal S_A according to the result of the comparison. For example, when a program address does not coincide with the bug address, the interrupt request signal S_A is held at a high level, while when the program address coincides with the bug address, the interrupt request signal S_A is held at a low level. The CPU 10 carries out the interrupt processing upon receiving the interrupt request signal ~~SA~~ S_A from the coincidence detecting circuit 120. For example, at the trailing edge of the interrupt request signal S_A, an interrupt request is generated for the CPU 10. The CPU 10 performs the interrupt processing after the end of the operation cycle of the instruction code being executed. That is, the coincidence of the program address with the predetermined bug address is detected by the coincidence detecting circuit 120, then the interrupt request signal S_A is held at the low level accordingly. The CPU 10 responds to the interrupt request at the trailing edge of the interrupt request signal S_A, suspends the program being executed, and carries out the interrupt processing. --

Please replace the paragraph beginning at page 24, line 21, with the following rewritten paragraph.

-- The coincidence detecting circuits 120-1 and 120-2 compare the two bug addresses with a program address. When addresses coincide, they output low level signals ~~SA1 and SA2~~ S_{A1} and S_{A2}, respectively. --

Please replace the paragraph beginning at page 24, line 25, with the following rewritten paragraph.

-- When there is sufficient leeway in the interrupt processing of the CPU 10, the output signals ~~SA1 and SA2~~ S_{A1} and S_{A2} of the coincidence detecting circuits 120-1 and 120-2 can be input to the CPU 10 as two different interrupt request signals. Accordingly, the CPU 10 receives these as different interrupt requests and executes the debugged programs separately to correct the two bugs. In general, however, the number of the interruptions that the CPU 10 is able to process is limited, so a plurality of bug processings ~~have~~ has to be assigned to a single interruption. In this case, as shown in FIG. 7, the output signals ~~SA1 and SA2~~ S_{A1} and S_{A2} of the coincidence detecting circuits 120-1 and 120-2 are input to an AND gate 130, and the output signal S_A ~~Of~~ of the AND gate 130 is input to the CPU 10 as the interrupt request signal. --